REMARKS

This is a full and timely response to the non-final Office Action of October 12, 2006. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this paper, claims 1, 2, 7, 8, 10, and 23-42 are pending in this application. Claims 23-28, 30-32, 35, 39, and 40 have been directly amended via the amendments set forth herein, and claims 41 and 42 are newly added. It is believed that the foregoing amendments add no new matter to the present application.

Response to §103 Rejections

In order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. See, *e.g.*, *In Re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* (U.S. Patent No. 6,446,107) in view of *Taewhan* ("Arithmetic Optimization using Carry-Save-Adders"). Claim 1 presently reads as follows:

> 1. An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:
>
> circuitry configured to receive at least a first operand, a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;
>
> a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and
>
> a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value and a carry value, wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output,
>
> wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, ***wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set***, wherein the propagate bit, if set, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if set, indicates that each of the bits of the respective coded logical value is set. (Emphasis added).

For at least the reasons set forth in the Amendment filed by Applicant on August 14, 2006, Applicant respectfully asserts that the cited art fails to suggest at least the features of claim 1 highlighted above. Therefore, the 35 U.S.C. §103 rejection of claim 1 is improper and should be withdrawn.

In addition, it is apparently alleged in the Office Action that, in *Knowles*, the outputs going to gates 24_0 and 24_1 (*i.e.*, the outputs of gate 10_0 and the exclusive OR gate that receives a_0 and b_0) constitute the "third propagate, kill, and generate recoded number representation" recited by claim 1. In this regard, it is alleged in the Office Action that *Knowles* discloses

> "a first adder (e.g. a mid portion of FIG. 3 including 8_0, 10_0, 8_1 logic gate and attached XOR gate which interfaces with all p, k, and g of a0-a1 and b0-b1) configured to add first operand (e.g. representations of a0 and b0) and second operand (e.g. representation of a1 and b1) to generate a third propagate, kill, and generate recoded number representation (e.g. outputs go to 24_0 and 24_1 logic gates)..."

However, there is nothing to indicate that such alleged output from the alleged "first adder" has a "kill bit," a "generate bit," and a "propagate bit," as defined by claim 1. Thus, the cited art fails to suggest at least the following features of claim 1:

> "a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation...
>
> wherein ***each*** of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, ***wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if set, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if set, indicates that each of the bits of the respective coded logical value is set.***" (Emphasis added).

For at least the above reasons, Applicant respectfully asserts that the cited art fails to teach each feature of claim 1. Therefore, the 35 U.S.C. §103 rejection of claim 1 should be withdrawn.

Claims 2, 23-25, 27-29, 33, 34, and 42

Claim 2 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view *Taewhan* and in view of *Miller* (U.S. Patent No. 5,706,323). Further, claims 23-25, 27-29, 33, and 34 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being anticipated by *Knowles* in view of *Taewhan*. In addition, claim 42 has been newly added via the amendments set forth herein. Applicant submits that the pending dependent claims 2, 23-25, 27-29, 33, 34, and 42 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2, 23-25, 27-29, 33, 34, and 42 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 1.

For example, claim 42 recites "wherein the first carry save adder is configured to set only a respective one of the propagate, kill and generate bits of the third propagate, kill, and generate recoded number representation for each possible state of the first and second propagate, kill, and generate recoded number representations." Applicant respectfully asserts that such features are not suggested by the cited art. Accordingly, claim 42 is allowable, notwithstanding the allowability of independent claim 1.

Claim 7

Claim 7 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan*. Claim 7 presently reads as follows:

> 7. A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:
>
> receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;
>
> generating a third propagate, kill, and generate representation and a carry-out value responsive to the first and second propagate, kill, and generate representations;
>
> logically combining the third propagate, kill, and generate representation with the carry-in value to generate a sum value and a carry value; and
>
> providing the carry-out value, the carry value, and the sum value as a result of the addition of the first and second propagate, kill, and generate representations,
>
> wherein ***each*** of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, ***wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if set, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if set, indicates that each of the bits of the respective coded logical value is set.*** (Emphasis added).

For at least reasons similar to those set forth hereinabove in the arguments for allowance of claim 1, Applicant respectfully asserts that the cited art fails to suggest at least the features of claim 7 highlighted above. Accordingly, the 35 U.S.C. §103 rejection of claim 7 is improper and should be withdrawn.

Claims 8, 10, 30, 32, 37, and 38

Claims 8, 30, 32, 37, and 38 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view of *Taewhan*. Further, claim 10 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan* and in view of *Miller*. Applicant submits that the pending dependent claims 8, 10, 30, 32, 37, and 38 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8, 10, 30, 32, 37, and 38 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 7.

Claim 35

Claim 35 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan*. Claim 35 presently reads as follows:

> 35. An apparatus for performing addition, said apparatus comprising:
> a first carry save adder configured to receive a first operand defining a first logical value encoded in propagate, kill, and generate (PKG) form such that the operand has a propagate bit, a generate bit, and a kill bit, the first carry save adder configured to receive a second operand defining a second logical value encoded in PKG form such that the second operand has a propagate bit, a generate bit, and a kill bit, ***the first carry save adder further configured to sum the first and second operands in PKG form to provide a first sum output in PKG form and a first carry bit without decoding the first and second operands from PKG form, the first sum output having a propagate bit, a generate bit, and a kill bit,***
> wherein the first carry bit and the propagate, generate, and kill bits of the first sum output collectively represent a summation of the first and second operands, wherein the first sum output represents a third logical value encoded in PKG form and equal to a sum of the first and second logical values, wherein the first logical

value has a plurality of bits, wherein the kill bit of the first operand, if set, indicates that none of the bits of the first logical value are set, wherein the propagate bit of the first operand, if set, indicates that only one of the bits of the first logical value is set, and wherein the generate bit of the first logical value, if set, indicates that each of the bits of the first logical value is set, wherein the second logical value has a plurality of bits, wherein the kill bit of the second operand, if set, indicates that none of the bits of the second logical value are set, wherein the propagate bit of the second operand, if set, indicates that only one of the bits of the second logical value is set, and wherein the generate bit of the second logical value, if set, indicates that each of the bits of the second logical value is set, wherein the third logical value has a plurality of bits, wherein the kill bit of the first sum output, if set, indicates that none of the bits of the third logical value are set, wherein the propagate bit of the first sum output, if set, indicates that only one of the bits of the third logical value is set, and wherein the generate bit of the first sum output, if set, indicates that each of the bits of the third logical value is set. (Emphasis added).

Applicant respectfully asserts that the alleged combination of *Knowles* and *Taewhan* fails to suggest at least the features of claim 35 highlighted hereinabove. Therefore, the 35 U.S.C. §103 rejection of claim 35 is improper and should be withdrawn.

In this regard, it is alleged in the Office Action that Figure 3 of *Knowles* depicts circuitry that adds an operand in PKG form. However, the outputs of Figure 3 are not in the "PKG form" described by claim 35, and Applicant submits that the cited art fails to suggest each feature of pending claim 35. Thus, the 35 U.S.C. §103 rejection of claim 35 should be withdrawn.

Claims 39-41

Claims 39 and 40 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view of *Taewhan*. Further, claim 41 has been newly added via the amendments set forth herein. Applicant submits that the pending dependent claims 39-41 contain all features of their respective independent claim 35. Since claim 35 should be allowed, as argued hereinabove, pending dependent claims 39-41 should be allowed as a matter of law for at

least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 35.

For example, claim 39 recites "wherein the first carry save adder is configured to set only a respective one of the kill, propagate, and generate bits of the first sum output regardless of the logical values defined by the operands." Applicant respectfully asserts that such features are not suggested by the cited art. Accordingly, the 35 U.S.C. §103 rejection of claim 39 is improper and should be withdrawn, notwithstanding the allowability of independent claim 35.

Allowable Subject Matter

Claims 26 and 31 have been indicated as allowable by the outstanding Office Action if such claims are rewritten to include the limitations of their respective base claims. For at least the reasons set forth hereinabove, Applicant submits that the respective base claims 1 and 7 are allowable and claims 26 and 31 are, therefore, allowable as a matter of law. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Accordingly, Applicant respectfully submits that claims 26 and 31 are allowable in their present form.

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

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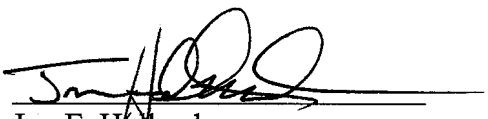
By: 

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